MB89352
SCSI Protocol Controller (SPC) with On-Chip Drivers/Receivers

Edition 1.0
September 1989

GENERAL DESCRIPTION

The MB89352 CMOS LSI SPC (SCSI Protocol Controller) is a circuit designed for easy control of the small computer system interface (SCSI).

The MB89352 can be used as a peripheral LSI circuit for an 8- or 16-bit MPU to realize high-level SCSI control. The SPC can control all the SCSI interface signals and handle almost all the interface control procedures. The on-chip driver/receivers allow for direct connection to the SCSI BUS.

This LSI circuit has an 8-byte FIFO data buffer register and a transfer byte counter that is 24 bits long. Furthermore, the MB89352 can serve as either an INITIATOR or a TARGET device for the SCSI, and can therefore be used for either an I/O controller or a host adapter.

SCSI Compatibility

- Full support for SCSI control (ANSI X3.1311986 Specification) except for synchronized transfer mode
- Serves as either INITIATOR or TARGET

Data Transfer Rate/Byte Counter

- 8-byte FIFO data timing control
- 24-bit transfer byte counter

Drive Options (on-chip driver/receiver)

- Single-ended

Selectable Transfer Modes

- DMA Transfer
- Program Transfer
- Manual Transfer

Clock Requirements

- 8 MHz clock

Technology/Power Requirements

- Silicon-gate CMOS
- Single +5 V power supply

Available Packaging

- 48-pin DIP or FLAT plastic packages

ABSOLUTE MAXIMUM RATINGS[1]

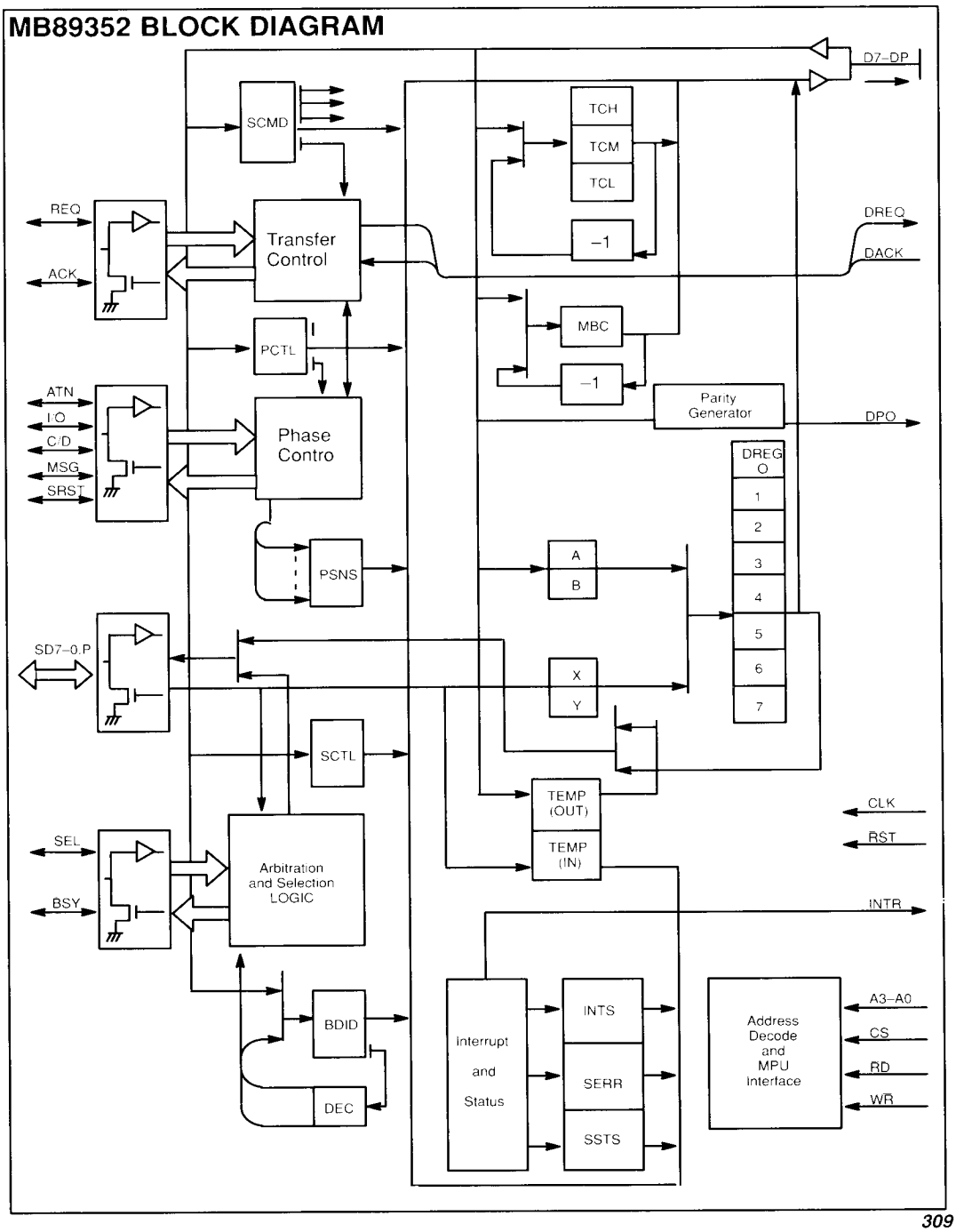
Rating	Designator	Values		Unit
		Min.	Max.	
Supply Voltage	V_{CC}	V_{SS} –0.3	7.0	V
Input Voltage	V_I	V_{SS} –0.3	7.3	V
Output Voltage[2]	V_O	V_{SS} –0.3	7.3	V
Storage Temperature	T_{STG}	–55	150	°C

Notes: 1 Permanent device damage may occur if the above absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2 Should not exceed V_{CC} + 0.5V.

RECOMMENDED OPERATING CONDITIONS

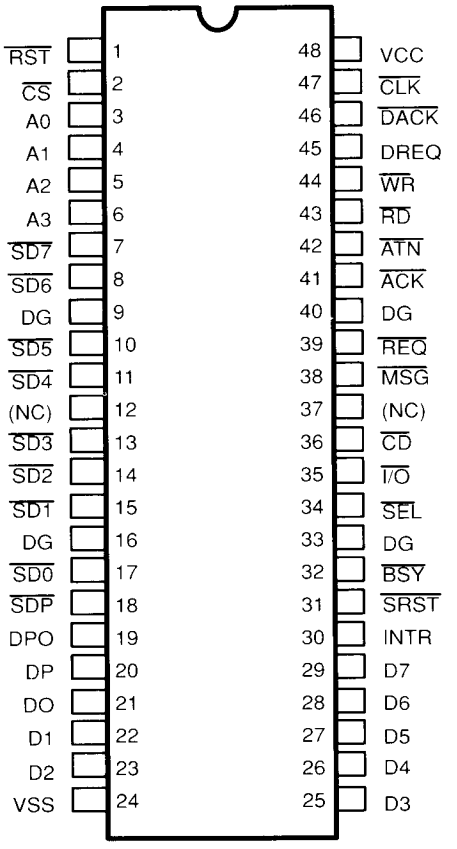
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Operating Ambient Temperature	T_A	0		+ 70	°C

MB89352 BLOCK DIAGRAM



PIN ASSIGNMENTS

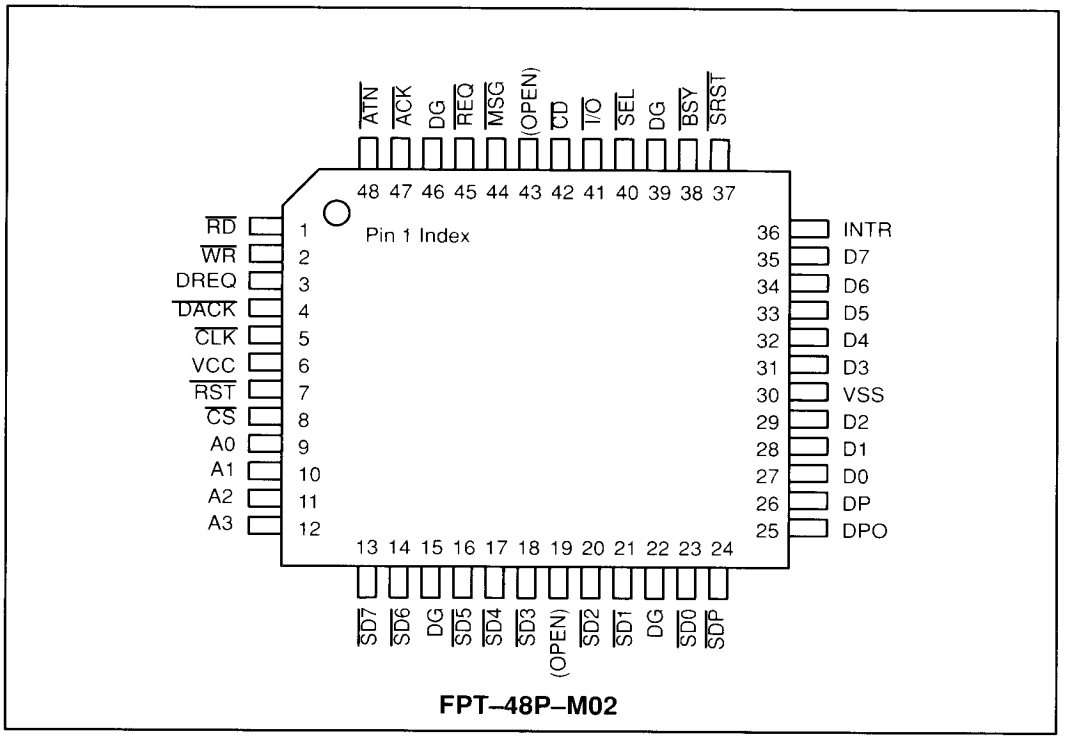
48-Pin Plastic DIP



DIP–48P–M02

PIN ASSIGNMENTS (Continued)

48-Pin Plastic Flat Package



FPT–48P–M02

PIN DESCRIPTIONS

Designator	Pin No.		I/O	Function
	DIP	FPT		
V_{CC}	48	6	—	+5V power supply.
V_{SS}	24	30	—	Circuit ground.
DG	9 16 33 40	15 22 39 46	—	Ground (OV) for internal drivers.The SCSI bus drivers can sink up to 48-mA each. Up to 16 drivers can be active at once. We recommend a good solid ground plane.
$\overline{CLK}$	47	5	I	Clock input for controlling internal operation and data transfer speed of the SPC.
$\overline{RST}$	1	7	I	Asynchronous reset signal used to clear all internal circuits of the SPC.
$\overline{CS}$	2	8	I	Input selection enable signal for accessing an internal register. When active low, the following input/output signals are valid: RD, WR, A3-A0, DP7-DP0 and DP.
A0 A1 A2 A3	3 4 5 6	9 10 11 12	I	Address input signals for selecting an internal register in SPC. MSB is A3; LSB is A0. When $\overline{CS}$ is active, read/ write is enabled for an internal register selected by these address inputs via data bus lines D0-D7 and DP.
$\overline{RD}$	43	1	I	This strobe input is used for reading out the contents of the SPC internal register, and is effective only when $\overline{CS}$ input is active. While $\overline{RD}$ is active, the contents of an internal register selected by A0 to A3 inputs are placed on data bus lines D7 to D0, DP. For a data transfer cycle in the program transfer mode, the rising edge of $\overline{RD}$ is used as a timing signal indicating the end of data read.
$\overline{WR}$	44	2	I	The strobe input is used for writing data into an SPC internal register, and is effective only when $\overline{CS}$ input is active. On the rising edge of this signal, data placed on data bus lines D0 to D7, DP are loaded into an internal register selected by A0 to A3 inputs. For a data transfer cycle in the program transfer mode, the rising edge of this signal is used as a timing signal indicating data ready status.
DP D0 D1 D2 D3 D4 D5 D6 D7	20 21 22 23 25 26 27 28 29	26 27 28 29 31 32 33 34 35	I/O	Used to write/read data to/from an internal register in the SPC. The data bus is 3-state and bidirectional.The MSB is D7 and the LSB is D0; DP is an odd parity bit. When both $\overline{CS}$ and RD inputs are active, the contents of a selected internal register are output to the data bus. In operations other than read/write, the data bus is kept at a high-Z level.

Continued on following page

PIN DESCRIPTIONS

Designator	Pin No.		I/O	Function
	DIP	FPT		
DPO	19	25	O	Outputs an odd parity of D0–D7. If parity bit is not generated for external memory, DPO can be used as an input parity bit for DP.
INTR	30	36	O	The INTR output signal is issued by the SPC and requests an interrupt to indicate completion of an internal operation or the occurrence of an error. Except for an interrupt caused by the RSTI input (reset condition in SCSI). When an interrupt request is granted, the INTR signal remains active until the interrupt is cleared.
DREQ	45	3	O	For a data transfer cycle in DMA mode. this signal isused to indicate a request for data transfer between the SPC and the external buffer memory. In an output operation, this signal becomes active to request a data transfer from the external buffer memory when the SPC internal data buffer register has free space available. In an input operation, it becomes active to request data transfer to the external buffer memory when the SPC internal data buffer resgister contains valid data.
$\overline{DACK}$	46	4	I	An active low response signal to the DREQ which request data transfer in between SPC and the external memory in the DMA mode. This signal in DMA mode functions similarly to the signal combination of $\overline{CS}$=low, A3=high, A2=low, A1–high, and A0=low (selection of DREG) in the program transfer mode. Since the DREG is selected by this $\overline{DACK}$ signal in the DMA mode instead of the address input from A3–A0, data transfer in between DREG of SPC and external memory is possible.
SD0 SD1 SD2 SD3 SD4 SD5 SD6 SD7 SDP	17 15 14 13 11 10 8 7 18	23 21 20 18 17 16 14 13 24	I/O	Active low bi–directional SCSI data bus. MSB : $\overline{SD7}$, LSB : $\overline{SD0}$ Odd parity bit : $\overline{SDP}$ Parity check for the SCSI data bus is programmable.
$\overline{SEL}$	34	40	I/O	A signal to issue or detect selection or reselection phase. In selection phase, an initiater asserts this signal, and in reselection phase the signal is asserted by the target.
$\overline{BSY}$	32	38	I/O	This signal indicates the SCSI bus use condition.This signal goes "L" when SPC is in arbitration phase or working as a target. Also, this signal is used to detect bus free phase with $\overline{SEL}$ signal.

Continued on following page

PIN DESCRIPTIONS

<table>
<tr><th rowspan="2">Designator</th><th colspan="2">Pin No.</th><th rowspan="2">I/O</th><th rowspan="2">Function</th></tr>
<tr><th>DIP</th><th>FPT</th></tr>
<tr><td>I/O
C/D
MSG</td><td>36
36
38</td><td>41
42
44</td><td>I/O</td><td>Signals to indicate actual phase of information transfer phase as follows:
MSG C/D I/O Phase Name
0 0 0 Data Out Phase
0 0 1 Data In Phase
0 1 0 Command Phase
0 1 1 Status Phase
1 0 0 Reserved
1 0 1 Reserved
1 1 0 Message Out Phase
1 1 1 Message In Phase
These signals are output from the target and initiator receives them always.</td></tr>
<tr><td>$\overline{REQ}$</td><td>39</td><td>45</td><td>I/O</td><td>In the data transfer phase, the REQ signal is used to notify the INITIATOR that the TARGET is ready to receive or send data. The REQ input is used as a timing control signal in the data transfer sequence.</td></tr>
<tr><td>$\overline{ACK}$</td><td>41</td><td>47</td><td>I/O</td><td>In the data transfer phase, the acknowledge signal is in response to a transfer request (REQ) signal from the TARGET. In the same way as REQ, an ACK input is used as a timing signal in the data transfer sequence.</td></tr>
<tr><td>$\overline{ATN}$</td><td>42</td><td>48</td><td>I/O</td><td>A signal to indicate attention condition. This signal is only output from an initiator.</td></tr>
<tr><td>$\overline{SRST}$</td><td>31</td><td>37</td><td>I/O</td><td>SCSI reset signal to be enabled by register setting. SCSI input from other SCSI devices is non-maskable.</td></tr>
<tr><td>NC</td><td>12, 37</td><td></td><td>—</td><td>Not connected</td></tr>
<tr><td>OPEN</td><td>—</td><td>19, 43</td><td></td><td>Reserved. (Do not make external connections to these pins)</td></tr>
</table>

ADDRESSING OF INTERNAL REGISTERS

SPC has internal registers, consisting of 15 bytes, that are accessible from an external circuit. These internal registers are used for controlling SPC internal operation and indicating SPC processing status/result status. A unique address is assigned to each internal register, and a particular register is identified by address bits A3 to A0. The following table shows internal register addressing:

Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select (CS)	Address Bits A3	A2	A1	A0
Bus Device ID	BDID	R	0	0	0	0	0
		W					
SPC Control	SCTL	R	0	0	0	0	1
		W					
Command	SCMD	R	0	0	0	1	0
		W					
Open	—	—	0	0	0	1	1
Interrupt Sense	INTS	R	0	0	1	0	0
Reset Interrupt		W					
Phase Sense	PSNS	R	0	0	1	0	1
SPC Diagnostic Control	SDGC	W					
SPC Status	SSTS	R	0	0	1	1	0
—		W					
SPC Error Status	SERR	R	0	0	1	1	1
—		W					
Phase Control	PCTL	R	0	1	0	0	0
		W					
Modified Byte Counter	MBC	R	0	1	0	0	1
—		W					

Continued on following page

Table 1. Internal Register Addressing

Register	Mnemonic	Operation	Chip Select ($\overline{CS}$)	Address Bits A3	A2	A1	A0
Data Register	DREG	R	0	1	0	1	0
		W					
Temporary Register	TEMP	R	0	1	0	1	1
		W					
Transfer Counter High	TCH	R	0	1	1	0	0
		W					
Transfer Counter Middle	TCM	R	0	1	1	0	1
		W					
Transfer Counter Low	TCL	R	0	1	1	1	0
		W					

BIT ASSIGNMENTS

The following table shows the bit assignments to each internal register. When accessing an internal register (in read/write), remember the following:

1. The internal register block includes the read–only/write–only register and those having different meanings in read and write operations.
2. A write command to a read–only register is ignored.
3. If the write–only register is read out, the data and parity bit are undefined.
4. At bit positions indicating "_" for a write in either 1 or 0 may be written.

Table 2. Bit Assignments for Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
0	Bus Device ID (BDID)	R	#7	#6	#5	#4	#3	#2	#1	#0	0
		W	— —					ID4	ID2	ID1	—
1	SPC Control (SCTL)	R/W	Reset & Disable	Control Reset	Diag Mode	ARBIT Enable	Parity Enable	Select Enable	Reselect Enable	INT Enable	P
2	Command (SCMD)	R	Command Code			RST Out	Intercept Xfer	Transfer Modifer PRG Xfer	0	Term Mode	P
		W									
3		R									
		W									
4	Interrupt Sense (SERR)	R	Selected	Reselected	Disconnect	Command Complete	Service Required	Time Out	SPC Hard Error	Reset Condition	P
		W	Reset Interrupt								—
5	Phase Sense (PSNS)	R	REQ	ACK	ATN	SEL	BSY	MSG	C/D	I/O	P
	SPC Diag. Control (SDGC)	W	Diag. REQ	Diag ACK	Xfer Enable		Diag. BSY	Diag. MSG	Diag. C/D	Diag. I/O	—
6	SPC Status (SSTS)	R	Connected INIT	Connected TARG	SPC BSY	XFER In Progress	SCSI RST	TC=0	DREG Status Full	DREG Status Empty	P
		W	—								—

Continued on following page

Bit Assignments For Internal Registers

HEX Address	Register and Mnemonic	R/W Operation	7 (MSb)	6	5	4	3	2	1	0 (LSb)	Parity
8	Phase Control (PCTL)	R	Bus Free Interrupt Enable	0				Transfer Phase			P
		W						MSG Out	C/D Out	I/O Out	
9	Modified Byte Counter (MBC)	R	0				MBC				P
							Bit 3	Bit 2	Bit 1	Bit 0	
		W	—							—	P
A	Data Register (DREG)	R	Internal Data Register (8 Byte FIFO)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
B	Temporary Register (TEMP)	R	Temporary Data (Input: From SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
		W	Temporary Data (Output: To SCSI)								
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P
C	Transfer Counter High (TCH)	R	Transfer Counter High (MSB)								
		W	Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16	P
D	Transfer Counter Mid (TCM)	R	Transfer Counter Middle (2nd Byte)								
		W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	P
E	Transfer Counter LOW (TCL)	R	Transfer Counter Low (LSB)								
		W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	P

These bit assignments for the MB89352 internal registers are identical to those in the MB87030, MB87031, and MB89351. Therfore, SPC replacement from one to another is very easy and does not require any new software design.

DC CHARACTERISTICS (T_A=0–70°C, V_{CC}=5V ±5%)

(Recommended operating conditions unless otherwise specified)

SCSI Bus Signal Pins

Parameter	Designator	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input High Voltage	V_{IH}		2.0	—	5.25	V
Input Low Voltage	V_{IL}		0	—	0.8	V
Input High Current	I_{IH}	V_{IH} + 5.25V	—	100	400	µA
Input Low Current	I_{IL}	V_{IL} + OV	—	–100	–400	µA
Output Low Voltage	V_{OL}	V_{CC} = 4.75V I_{OL} + 48mA	—	—	0.5	V
Input Hysteresis Width	V_{HM}	—	0.2	0.4	—	V

DC CHARACTERISTICS (Continued)

MPU Bus Signal Pins

Parameter	Designator	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input High Voltage	V_{IH}		2.2	—	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} −0.3	—	0.8	V
Output High Voltage	V_{OH}	I_{OH} + 0.4 mA	4.0		V_{CC}	V
Output Low Voltage	V_{OL}	I_{OL} + 3.2 mA	V_{SS}		0.4	V
Input Leakage Current	I_{LIH}	V_{IH} + 5.25			20	µA
	I_{LIL}	V_{IL} + 0.0			−10	µA
Input/Output Leakage Current	I_{LZH}	V_{IH} + 5.25			40	µA
	I_{LZL}	V_{IL} + 0.0			−40	µA
Power Supply Current	I_{CC}	Input Clock = 8 MHz All Output Pins Open			10	mA

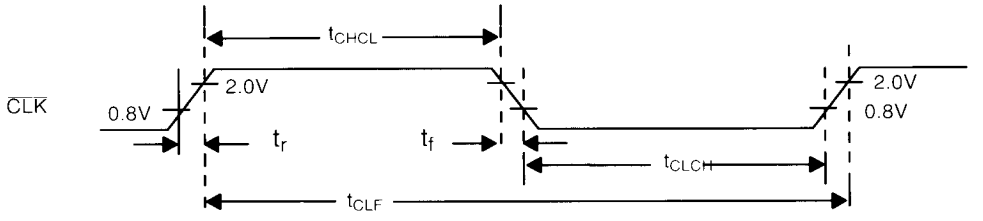
AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted)

Clock Signal

$\overline{CLK}$ Input					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{CLK}$ Cycle Time	t_{CLF}	125		200	ns
$\overline{CLK}$ High Time	t_{CHCL}	44			ns
$\overline{CLK}$ Pulse Width	t_{CLCH}	44			ns
$\overline{CLK}$ Rising Skew Time	t_r			10	ns
$\overline{CLK}$ Falling Skew Time	t_f			10	ns

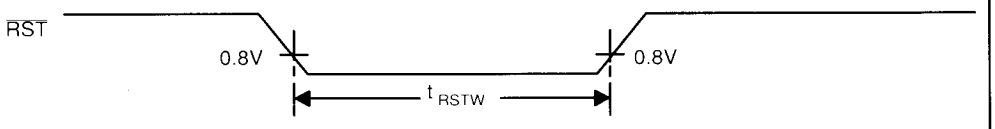
Clock Signal Timing



AC CHARACTERISTICS (Continued)

RST Input					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{RST}$ Pulse Width	t_{RSTW}	100			ns

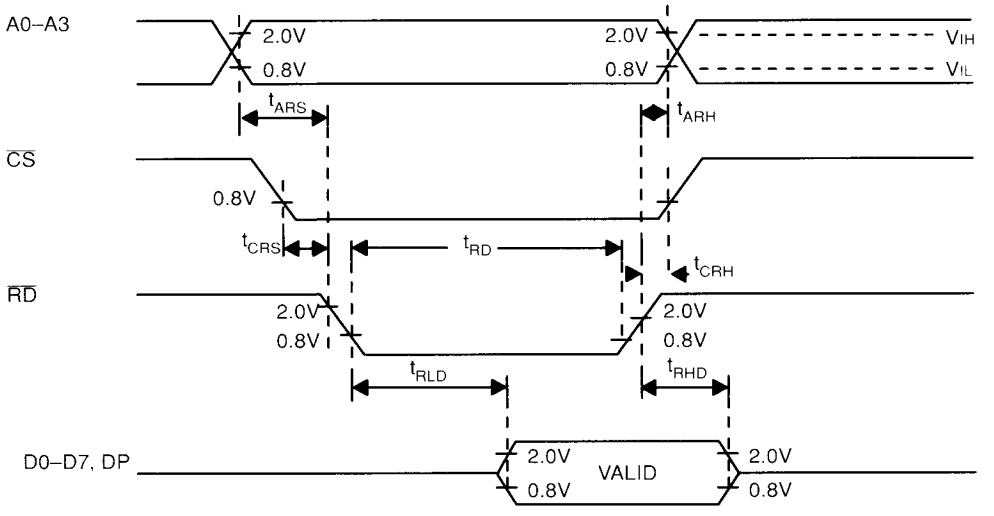
Reset Input Timing



AC CHARACTERISTICS (Continued)

Register Read					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Address Setup Time	t_{ARS}	40			ns
Address Hold Time	t_{ARH}	10			ns
$\overline{CS}$ Setup Time	t_{CRS}	25			ns
$\overline{CS}$ Hold Time	t_{CRH}	10			ns
Data Valid Time (from $\overline{RD}$ Low) (C_L = 80pF)	t_{RLD}			90	ns
Data Valid Time (from $\overline{RD}$ Hi gh) (C_L = 20pF)	t_{RHD}	10		60	ns
$\overline{RD}$ Pulse Width	t_{RD}	120			ns

Register Read Timing

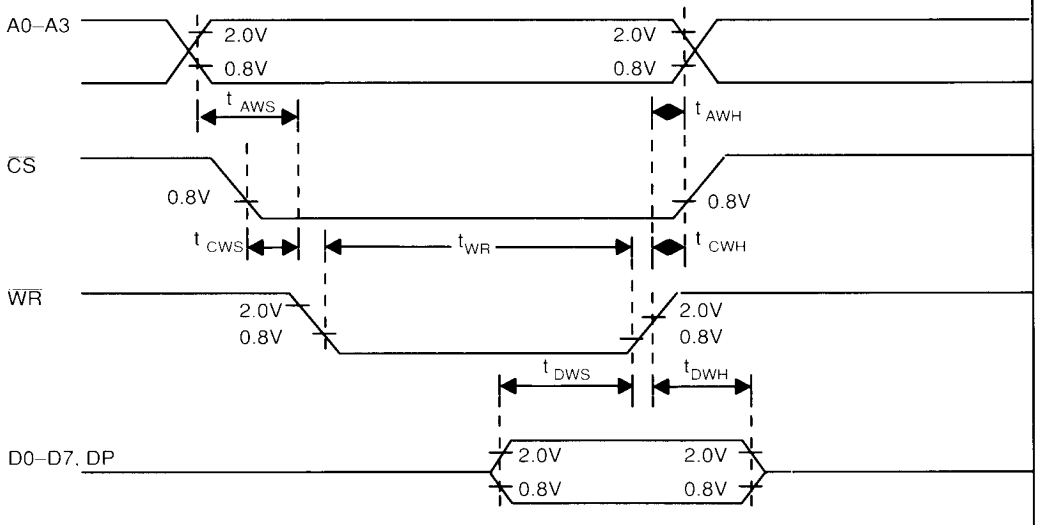


AC CHARACTERISTICS (Continued)

Register Write

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Address Setup Time	t_{AWS}	40			ns
Address Hold Line	t_{AWH}	10			ns
$\overline{CS}$ Setup Time	t_{CWS}	25			ns
$\overline{CS}$ Hold Time	t_{CWH}	10			ns
Data Bus Setup Time	t_{DWS}	30			ns
Data Bus Hold Time	t_{DWH}	20			ns
WR Pulse Width	t_{WR}	100			ns

Register Write Timing

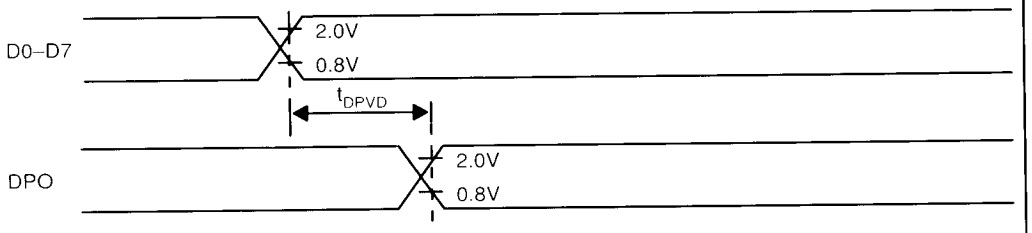


AC CHARACTERISTICS (Continued)

DPO (Data Parity Output)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
Data Bus (D0 – D7) Valid to DPO Valid	t_{DPVD}	CL = 30pF			60	ns

DPO Timing



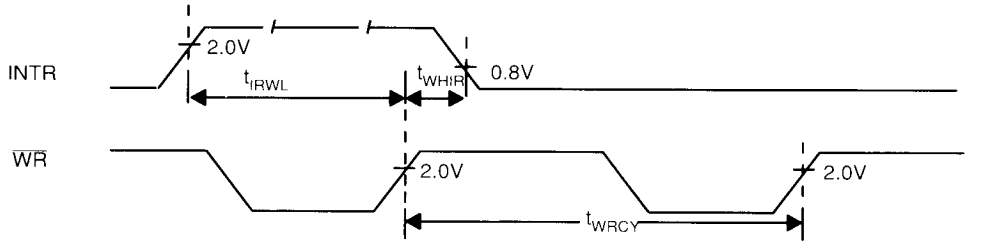
AC CHARACTERISTICS (Continued)

INTR (Interrupt Request) Output

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$\overline{WR}$ High to INTR Low (Interrupt reset)	t_{WHIR}	CL = 10pf	t_{CLF}		$2t_{CLF} + 100$	ns
INTR High to $\overline{WR}$ High	t_{IRWL}		0			ns
INTR Reset Cycle Time[1]	t_{WRCY}		$4t_{CLF}$			ns

Note: [1]Applicable only when interrupt reset is executed.

Interrupt Output Timing



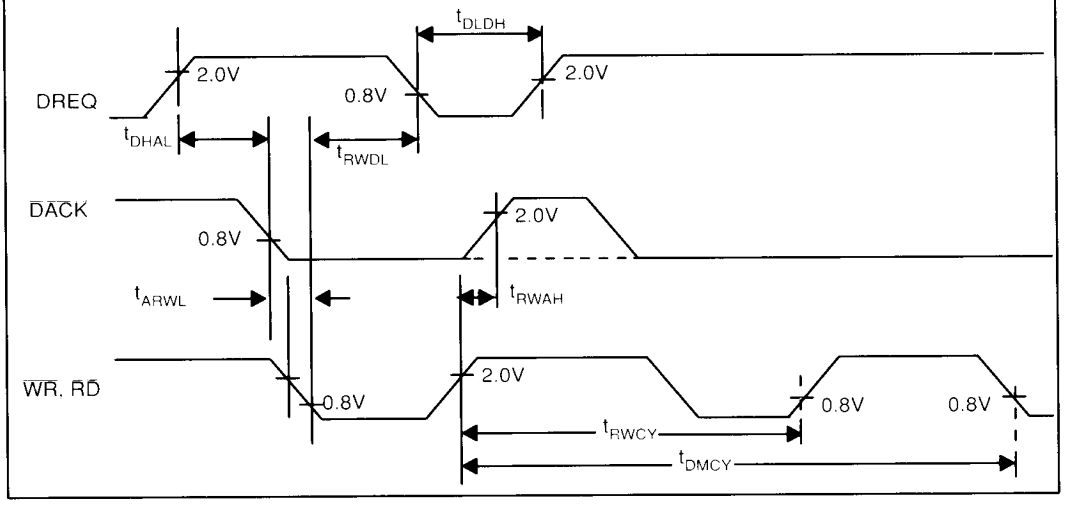
AC CHARACTERISTICS (Continued)

DMA Access

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
DREQ High to $\overline{DACK}$ Low	t_{DHAL}		0			ns
$\overline{WR}$ and $\overline{RD}$ Service Time (From $\overline{DACK}$ Low to $\overline{WR}$ or $\overline{RD}$ Low)	t_{ARWL}		40			ns
DREQ Release Time (From $\overline{WR}$ or $\overline{RD}$ Low to DREQ Low)[1]	t_{RWDL}	CL = 30 pF	35		150	ns
DACK Hold Time (From $\overline{WR}$ or $\overline{RD}$ High to $\overline{DACK}$ Low)	t_{RWAH}		10			ns
DREG Interval (From DREQ Low to DREQ High)	t_{DLDH}		0			ns
DREG Access Cycle Time (1)	t_{RWCY}		$2t_{CLF}$			ns
DREG Access Cycle Time (2)	t_{DMCY}		$3t_{CLF}$			ns

Note: 1 The $\overline{WR}$ parameter is applicable when the data buffer register is full; the $\overline{RD}$ parameter is applicable when the data buffer register is empty.

DMA Access Timing

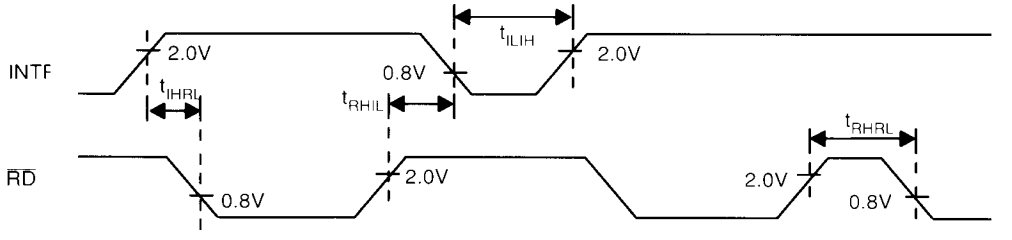


AC CHARACTERISTICS (Continued)

DREG Access – Program Transfer with INTR (Input Operation)						
Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$\overline{RD}$ Service Time (From INTR High to $\overline{RD}$ Low)	t_{IHRL}		0			ns
INTR Release Time (From $\overline{RD}$ High to INTR Low) (Note)	t_{RHIL}	CL = 20 pF	35		150	ns
INTR Recovery Time (From INTR Low to INTR High)	t_{ILIH}		0			ns
$\overline{RD}$ Recovery Time (From $\overline{RD}$ High to $\overline{RD}$ Low)	t_{RHRL}		50			ns

Note: This parameter is applicable when the data buffer register is full in the output operation and empty in the input operation.

DREG Access Timing (Input Operation)



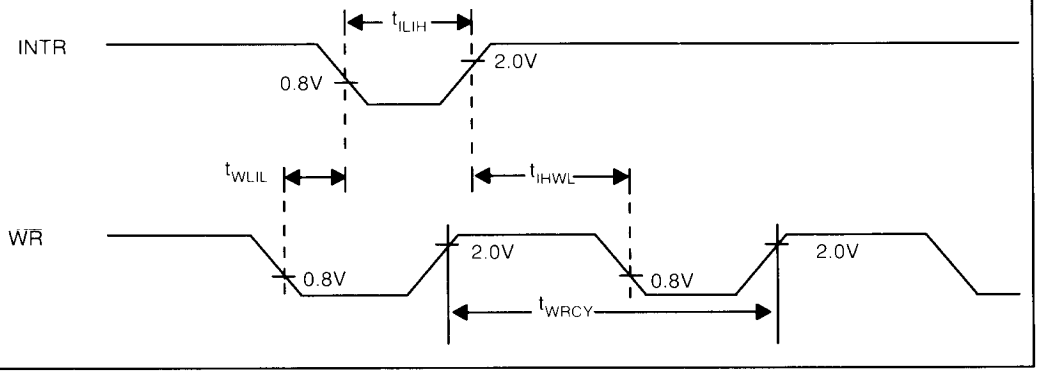
AC CHARACTERISTICS (Continued)

DREG Access – Program Transfer with INTR (Output Operation)

Parameter	Designator	Test Conditions	Values			Unit
			Min.	Typ.	Max.	
$\overline{WR}$ Service Time (From INTR High to $\overline{WR}$ Low)	t_{IHWL}		0			ns
INTR Release Time (From $\overline{WR}$ High to INTR Low) (Note)	t_{WLIL}	CL = 20 pF	35		150	ns
INTR Recovery Time (From $\overline{WR}$ Low to INTR High)	t_{ILIH}		0			ns
$\overline{WR}$ Cycle Time	t_{WRCY}		$2t_{CLF}$			ns

Note: This parameter is applicable when the data buffer register is full in the output operation and empty in the input operation.

DREG Access Timing (Output Operations)



AC CHARACTERISTICS (Continued)

SCSI Bus Interface Selection Phase Timing

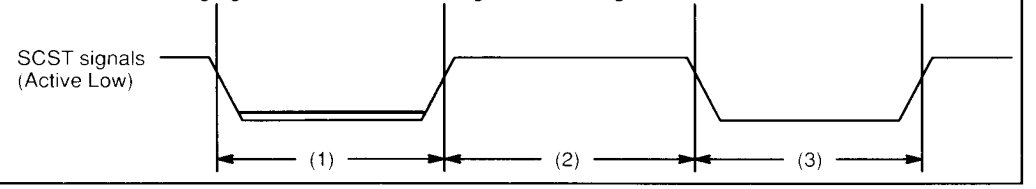
INITIATOR — Selection With Arbitration

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Bus Free Time*	t_{BFR}	$4t_{CLF}+50$			ns
Start of Arbitration	t_{BFBL}	$(6+n)^{**} \times t_{CLF}$		$(7+n) \times t_{CLF}+60$	ns
$\overline{BSY}$ Low to Self ID# Output	t_{BLID}	0		60	ns
$\overline{BSY}$ Low to Prioritize	t_{ARB}	$32t_{CLF}-60$			ns
Data Bus Valid to Prioritize	t_{AIDV}	200			ns
Bus Usage Permission Granted to $\overline{SEL}$ Low	t_{AWSL}	0		80	ns
$\overline{SEL}$ Low to Data Bus ID Output, $\overline{ATN}$ Low	t_{SIDA}	$11t_{CLF}-30$			ns
Select ID# Output to $\overline{BSY}$ High	t_{IDBH}	$2t_{CLF}-80$			ns
$\overline{BSY}$ Low to $\overline{SEL}$ High	t_{BLSH}	$2t_{CLF}$			ns
$\overline{BSY}$ Low to Select ID# Hold	t_{BIDH}	$2t_{CLF}$			ns
$\overline{SEL}$ High to INTR High	t_{SHIR}			60	ns
$\overline{SEL}$ Low to $\overline{BSY}$ High, ID Bit High	t_{SBCR}			$3t_{CLF}+180$	ns
Prioritize to $\overline{BSY}$ High, ID Bit High	t_{PBCR}			110	ns

Notes: *Bus Free Time : The minimum time period until the booked select command is executed.
**TCL register value.

All SCSI Timing Signals

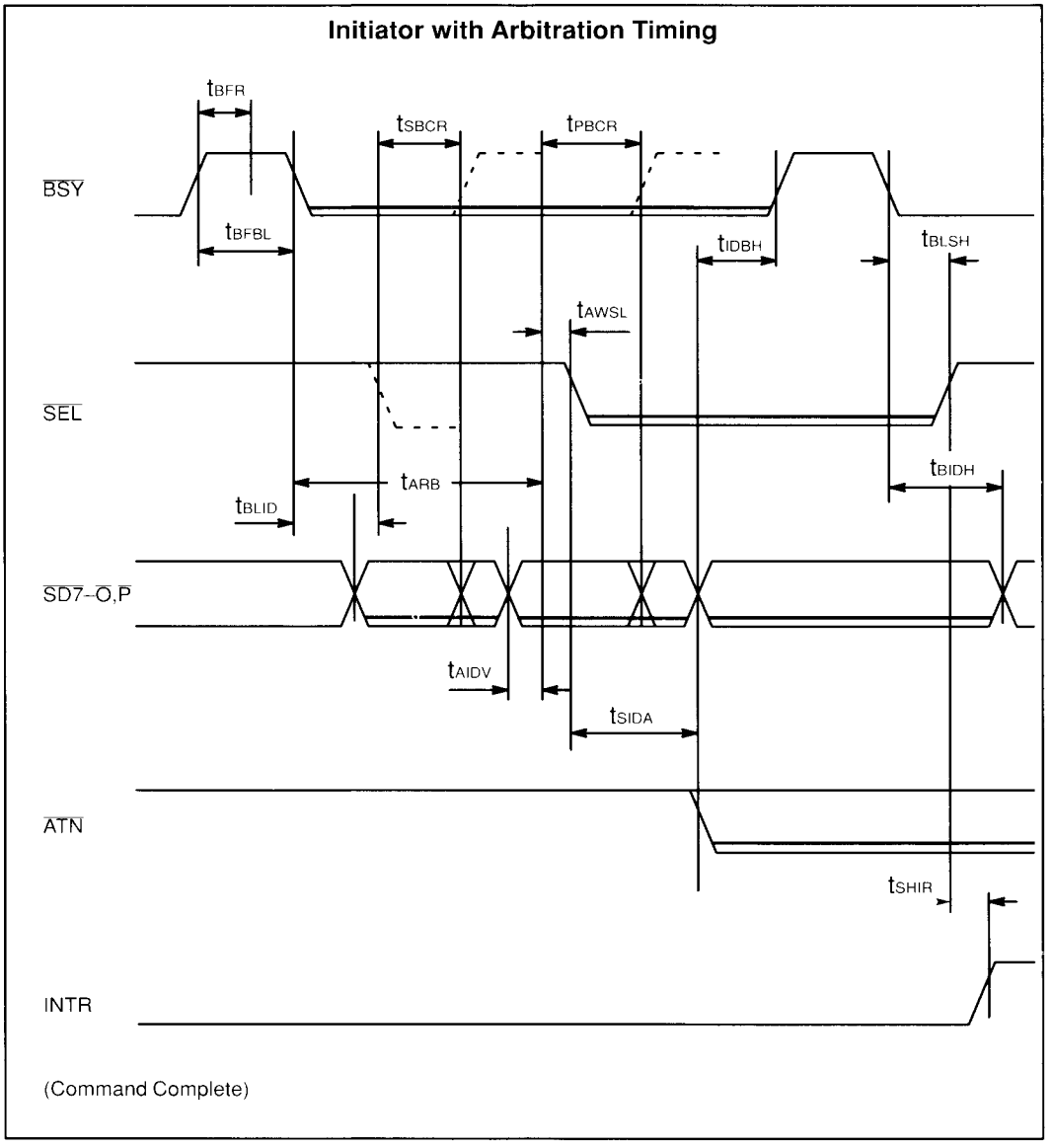
Note: All SCSI timing signals are defined according to the following rules:



Notes: (1) The SPC outputs low level signal to the bus.
(2) All devices hooked up to the bus do not output low level signals.
(3) Other devices hooked up to the bus output low level signals.

AC CHARACTERISTICS (Continued)

SCSI Bus Interface Selection Phase Timing



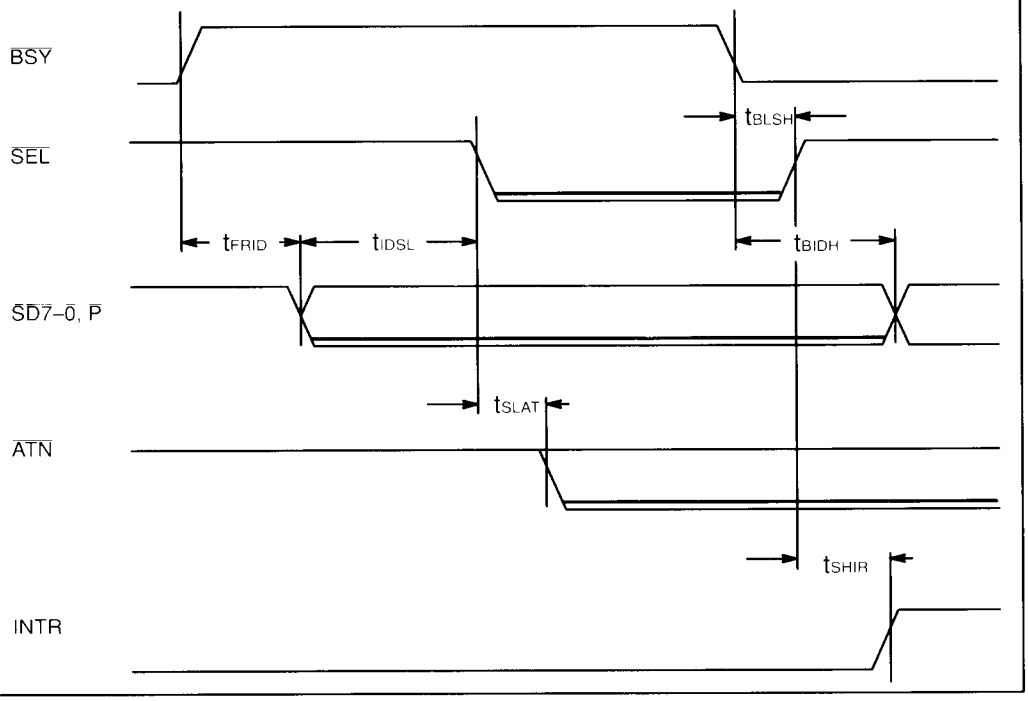
AC CHARACTERISTICS (Continued)

INITIATOR — Selection Without Arbitration

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{BSY}$ High to Select ID# Output	t_{FRID}	(6+n) x t_{CLF}		(7+n) x t_{CLF}+140	ns
ID# Output to $\overline{SEL}$ Low	t_{IDSL}	11t_{CLF}–80			ns
$\overline{SEL}$ Low to $\overline{ATN}$ Low	t_{SLAT}	11t_{CLF}–80			ns
$\overline{BSY}$ Low to $\overline{SEL}$ High	t_{BLSH}	2t_{CLF}			ns
$\overline{BSY}$ Low to ID# Hold	t_{BIDH}	2t_{CLF}			ns
$\overline{SEL}$ High to INTR High	t_{SHIR}			60	ns

Note: n=TCL register set value.

Initiator Without Arbitration Timing

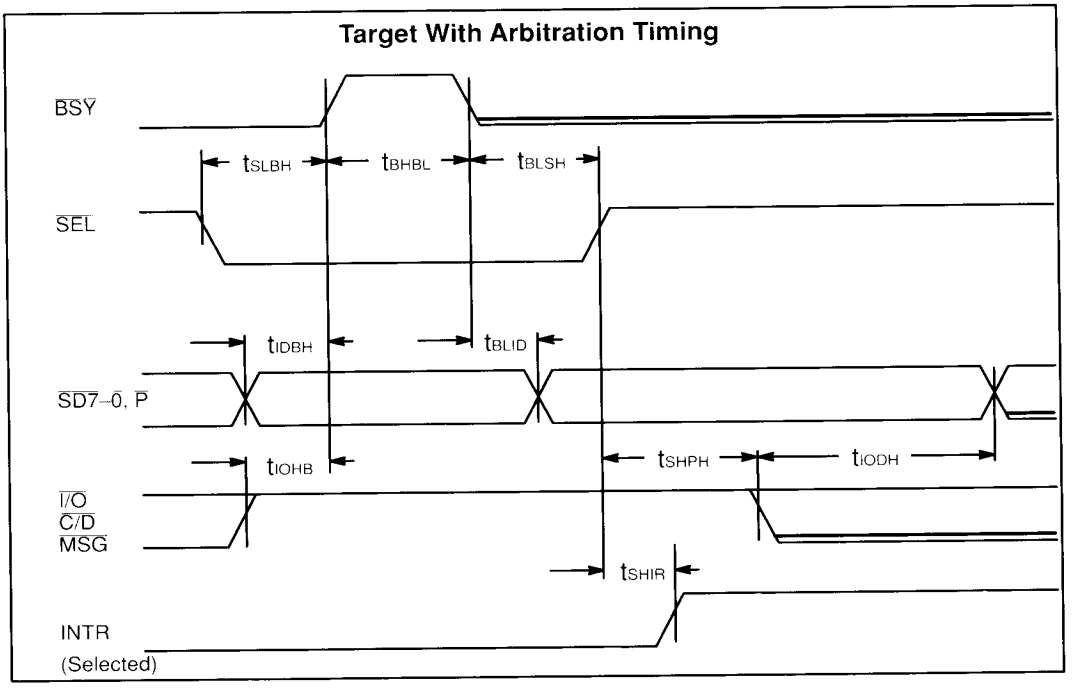


AC CHARACTERISTICS (Continued)

TARGET — Selection With Arbitration

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{SEL}$ Low to $\overline{BSY}$ High	t_{SLBH}	0			ns
Data Bus Valid (ID#) to $\overline{BSY}$ High	t_{IDBH}	0			ns
$\overline{I/O}$ High to $\overline{BSY}$ High	t_{IOHB}	0			ns
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{BHBL}	$4t_{CLF}$		$5t_{CLF}+140$	ns
$\overline{BSY}$ Low to ID# Hold	t_{BLID}	60			ns
$\overline{BSY}$ Low to $\overline{SEL}$ High	t_{BLSH}	0			ns
$\overline{SEL}$ High to Phase Signal Output	t_{SHPH}	$3t_{CLF}$		$4t_{CLF}+160$	ns
$\overline{I/O}$ Low to Data Bus Output	t_{IODE}	$7t_{CLF}$			ns
$\overline{SEL}$ High to INTR High	t_{SHIR}			$3t_{CLF}+130$	ns

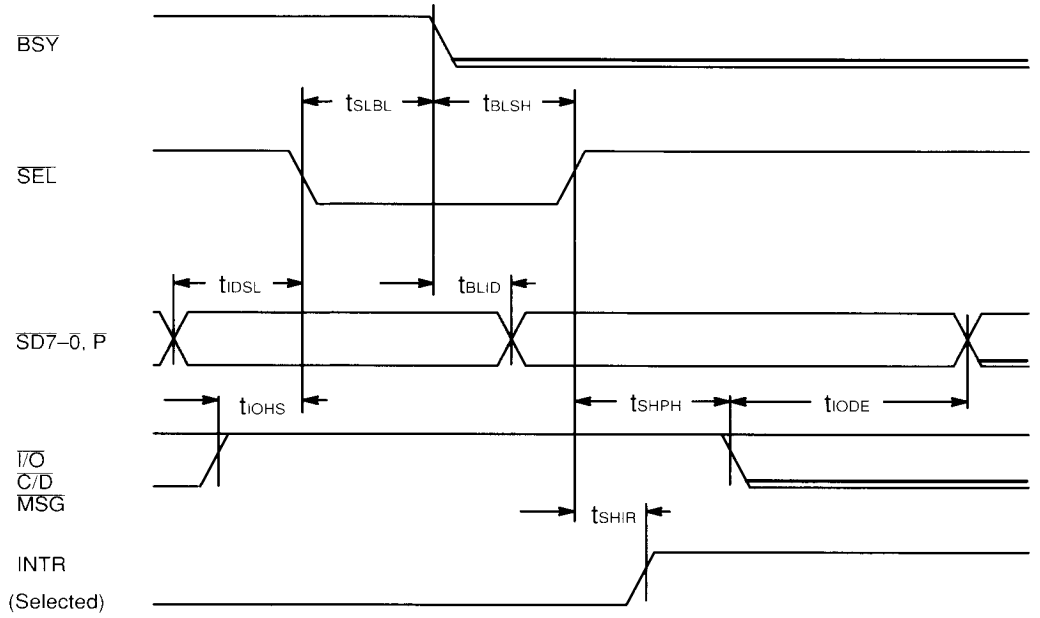
Target With Arbitration Timing



AC CHARACTERISTICS (Continued)

TARGET — Selection Without Arbitration					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Data Bus Valid (ID#) to $\overline{SEL}$ Low	t_{IDSL}	0			ns
$\overline{I/O}$ High to $\overline{SEL}$ Low	t_{IOHS}	0			ns
$\overline{SEL}$ Low to $\overline{BSY}$ Low	t_{SLBL}	$2t_{CLF}$		$3t_{CLF}+130$	ns
$\overline{BSY}$ Low to ID# Hold	t_{BLID}	60			ns
$\overline{BSY}$ Low to $\overline{SEL}$ High	t_{BLSH}	0			ns
$\overline{SEL}$ High to Phase Signal Output	t_{SHPH}	$3t_{CLF}$		$4t_{CLF}+160$	ns
I/O Low to Data Bus Output	t_{IODE}	$7t_{CLF}$			ns
$\overline{SEL}$ High to INTR High	t_{SHIR}			$3t_{CLF}+130$	ns

Target Without Arbitration Timing



AC CHARACTERISTICS (Continued)

SCSI BUS INTERFACE – RESELECTION PHASE TIMING

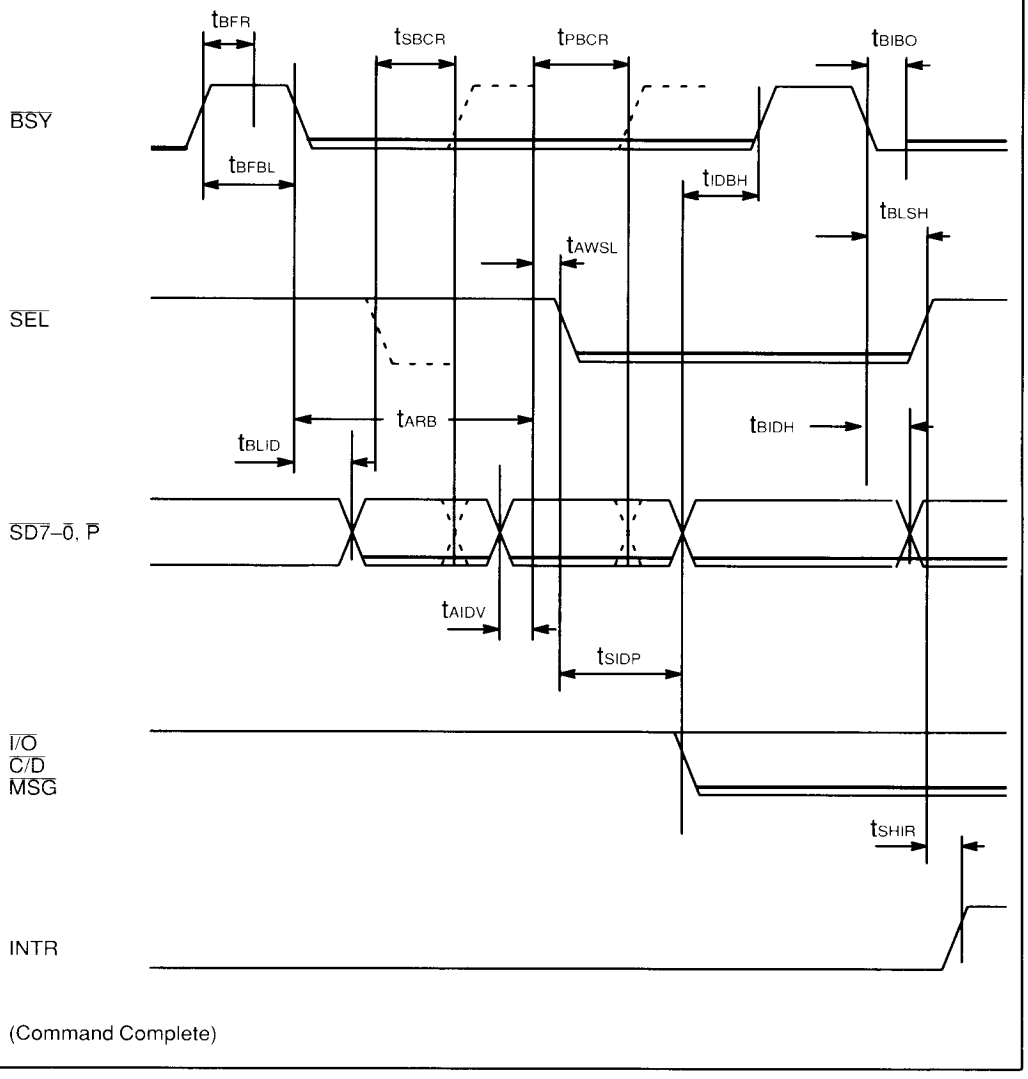
TARGET — Reselection Phase Timing

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
Bus Free Time*	t_{BFR}	$4t_{CLF}+50$			ns
Start of Arbitration	t_{BFBL}	$(6+n)^{**} \times t_{CLF}$		$(7+n) \times t_{CLF}+140$	ns
$\overline{BSY}$ Low to Self ID# Output	t_{BLID}	0		60	ns
$\overline{BSY}$ Low to Prioritize	t_{ARB}	$32t_{CLF}-60$			ns
Data Bus Valid to Prioritize	t_{AIDV}	200			ns
Bus Usage Permission Granted to $\overline{SEL}$ Low	t_{AWSL}	0		80	ns
$\overline{SEL}$ Low to Data Bus ID Output, Phase Signal Output	t_{SIDP}	$11t_{CLF}-50$			ns
Select ID# Output to $\overline{BSY}$ High	t_{IDBH}	$2t_{CLF}-80$			ns
$\overline{BSY}$ Low to $\overline{BSY}$ Low Output	t_{BIBO}	$2t_{CLF}+20$		$3t_{CLF}+140$	ns
$\overline{BSY}$ Low to $\overline{SEL}$ High	t_{BLSH}	$2t_{CLF}$			ns
$\overline{BSY}$ Low to Select ID# Hold	t_{BIDH}	$2t_{CLF}$			ns
$\overline{SEL}$ High to INTR High	t_{SHIR}			60	ns
$\overline{SEL}$ Low to $\overline{BSY}$ High, ID Bit High	t_{SBCR}			$3t_{CLF}+180$	ns
Prioritize to $\overline{BSY}$ High, ID Bit High	t_{PBCR}			110	ns

Notes: *Bus Free Time:=The minimum time period till the booked select command is executed.
**n=TCL register value

AC CHARACTERISTICS (Continued)

Reselection Timing (Target)

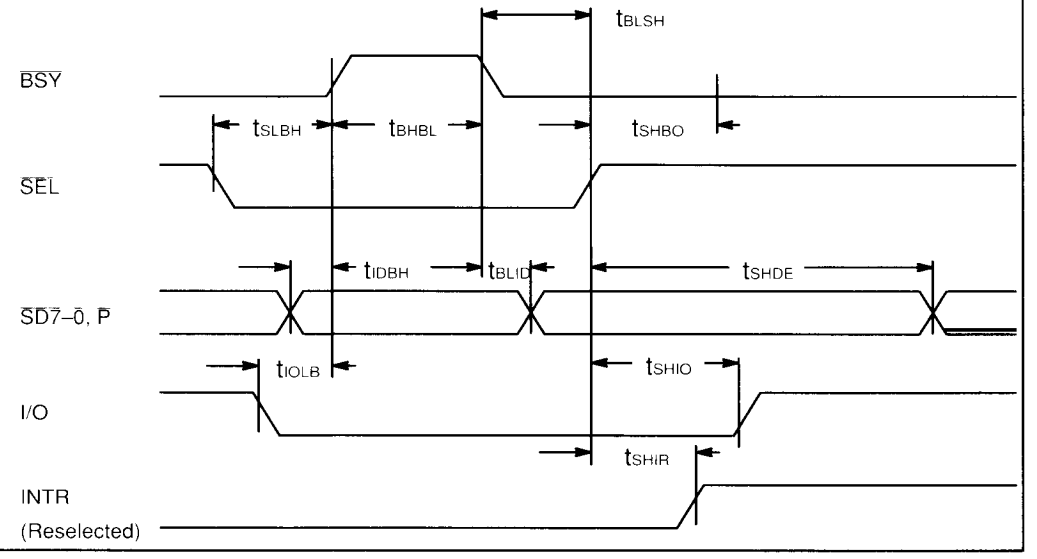


AC CHARACTERISTICS (Continued)

INITIATOR — Reselection Phase Timing

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{SEL}$ Low to $\overline{BSY}$ High	t_{SLBH}	0			ns
Data Bus Valid (ID#) to $\overline{BSY}$ High	t_{IDBH}	0			ns
$\overline{I/O}$ Low to $\overline{BSY}$ High	t_{IOLB}	0			ns
$\overline{BSY}$ High to $\overline{BSY}$ Low	t_{BHBL}	$4t_{CLF}$		$5t_{CLF}+140$	ns
$\overline{BSY}$ Low to ID# Hold	t_{BLID}	60			ns
$\overline{BSY}$ Low to $\overline{SEL}$ High	t_{BLSH}	0			ns
$\overline{SEL}$ High to $\overline{BSY}$ Low Output	t_{SHBO}	$2t_{CLF}$		$3t_{CLF}+140$	ns
$\overline{SEL}$ High to Data Bus Valid (When $\overline{I/O}$ is High)	t_{SHDE}	$3t_{CLF}+30$		$4t_{CLF}+160$	ns
$\overline{SEL}$ High to $\overline{I/O}$ High	t_{SHIO}	200			ns
$\overline{SEL}$ High to INTR High	t_{SHIR}			$3t_{CLF}+130$	ns

Reselection Timing (Initiator)



AC CHARACTERISTICS (Continued)

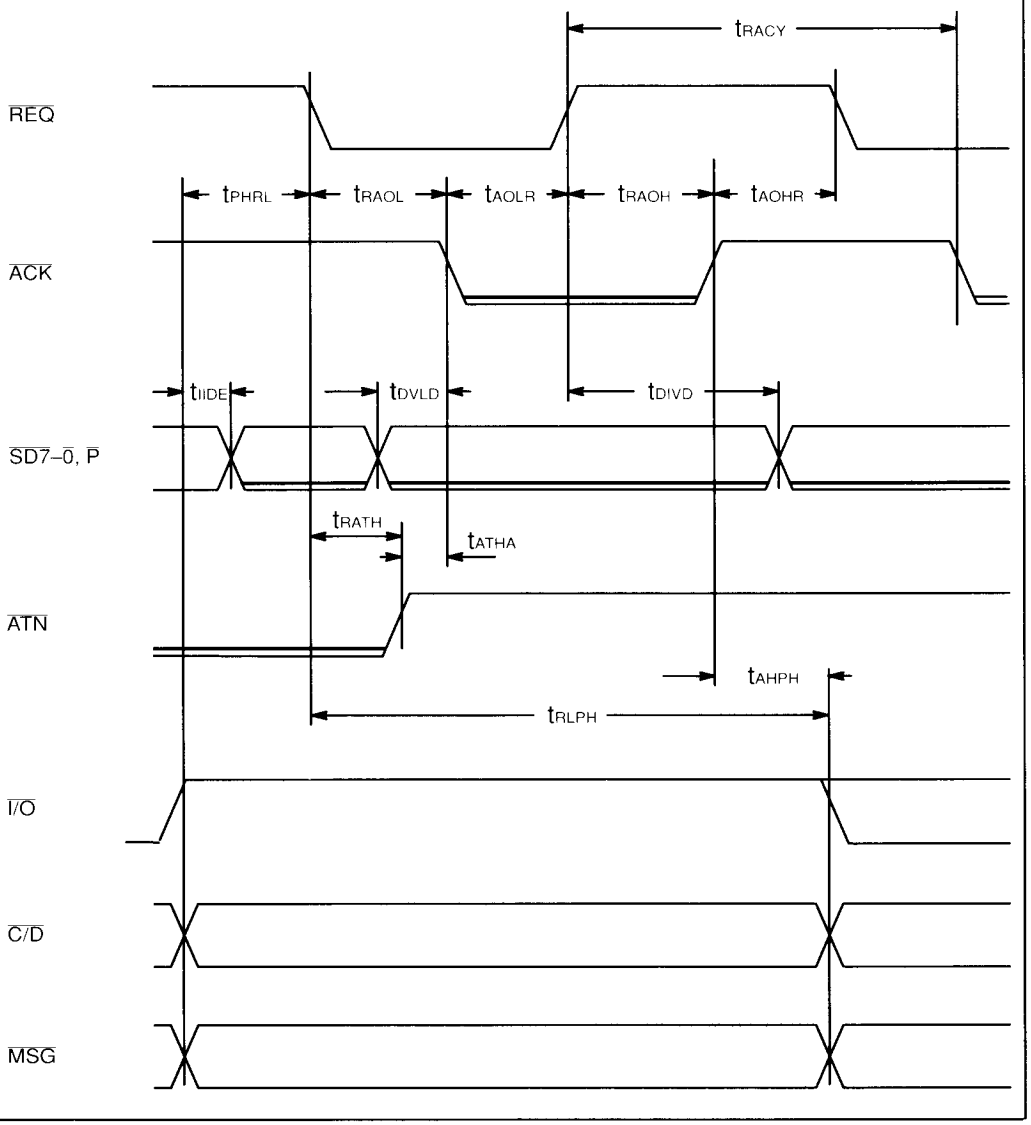
SCSI BUS INTERFACE – INFORMATION TRANSFER PHASE TIMING

INITIATOR —Asynchronous Transfer Output					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{I/O}$ High to Data Bus Output	t_{IIDE}	10			ns
Phase Set to $\overline{REQ}$ Low	t_{PHRL}	100			ns
$\overline{REQ}$ Low to $\overline{ACK}$ Low	t_{RAOL}	20			ns
Data Bus Valid to $\overline{ACK}$ Low	t_{DVLD}	$2t_{CLF}-80$			ns
$\overline{ACK}$ Low to $\overline{REQ}$ High	t_{AOLR}	0			ns
$\overline{REQ}$ High to $\overline{ACK}$ High	t_{RAOH}	10			ns
$\overline{ACK}$ High to $\overline{REQ}$ Low	t_{AOHR}	0			ns
$\overline{REQ}$ High to $\overline{ACK}$ Low	t_{RACY}	$2t_{CLF}$			ns
$\overline{REQ}$ High to Data Bus Hold	t_{DIVD}	15			ns
$\overline{REQ}$ Low to $\overline{ATN}$ High[1]	t_{RATH}	$2t_{CLF}$			ns
$\overline{ATN}$ High to $\overline{ACK}$ Low[1]	t_{ATHA}	$t_{CLF}-20$			ns
$\overline{REQ}$ Low to Phase Change[2]	t_{RLPH}	$3t_{CLF}$			ns
$\overline{ACK}$ High to Phase Change[2]	t_{AHPH}	10			ns

Notes: 1 This spec is applicable to the last byte transfer of message out phase in hardware transfer mode.
2 When the transfer phase is changed. both t_{RLPH} and t_{ALPH} should be specified.

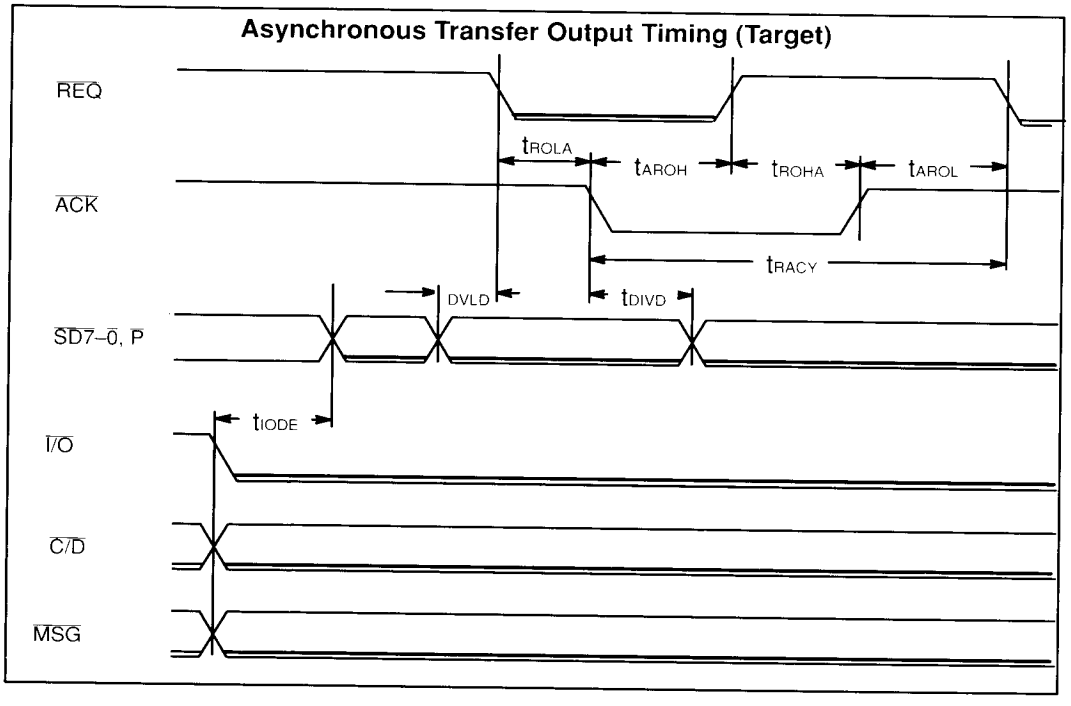
AC CHARACTERISTICS (Continued)

Asynchronous Transfer Output Timing (Initiator)



AC CHARACTERISTICS (Continued)

TARGET —Asynchronous Transfer Output					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{I/O}$ Low to Data Bus Output	t_{IODE}	$7t_{CLF}$			ns
Data Bus Valid to $\overline{REQ}$ Low	t_{DVLD}	$2t_{CLF}-80$			ns
$\overline{ACK}$ Low to Data Bus Hold	t_{DIVD}	15			ns
$\overline{REQ}$ Low to $\overline{ACK}$ Low	t_{ROLA}	0			ns
$\overline{ACK}$ Low to $\overline{REQ}$ High	t_{AROH}	10		180	ns
$\overline{REQ}$ High to $\overline{ACK}$ High	t_{ROHA}	0			ns
$\overline{ACK}$ High to $\overline{REQ}$ Low	t_{AROL}	10			ns
$\overline{ACK}$ Low to $\overline{REQ}$ Low	t_{RACY}	$2t_{CLF}$			ns



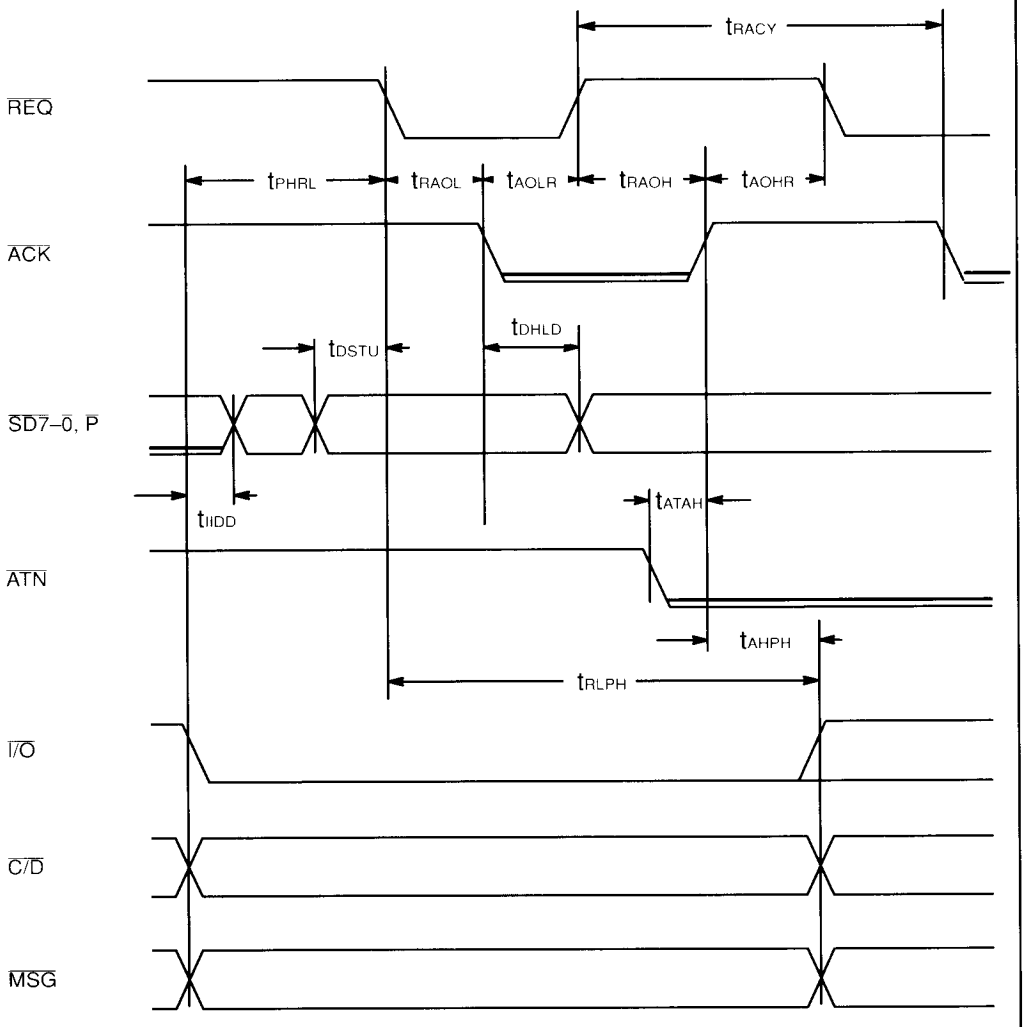
AC CHARACTERISTICS (Continued)

INITIATOR —Asynchronous Transfer Input					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{I/O}$ Low to Data Bus Output Terminate	t_{IIDD}			140	ns
Phase Set to $\overline{REQ}$ Low	t_{PHRL}	100			ns
Data Bus Valid to $\overline{REQ}$ Low	t_{DSTU}	10			ns
$\overline{REQ}$ Low to $\overline{ACK}$ Low	t_{RAOL}	20			ns
$\overline{ACK}$ Low to $\overline{REQ}$ High	t_{AOLR}	0			ns
$\overline{ACK}$ Low to Data Bus Hold	t_{DHLD}	15			ns
$\overline{REQ}$ High to $\overline{ACK}$ High	t_{RAOH}	10			ns
$\overline{ACK}$ High to $\overline{REQ}$ Low	t_{AOHR}	0			ns
$\overline{REQ}$ High to $\overline{ACK}$ Low	t_{RACY}	$2t_{CLF}$			ns
$\overline{ATN}$ Low to $\overline{ACK}$ High[1]	t_{ATAH}	$t_{CLF}-20$			ns
$\overline{REQ}$ Low to Phase Change[2]	t_{RLPH}	$3t_{CLF}$			ns
$\overline{ACK}$ High to Phase Change[2]	t_{AHPH}	10			ns

Notes: 1 Applicable to the last byte transfer of message out phase in hardware transfer mode.
2 When the transfer phase is changed, both t_{RLPH} and t_{AHPH} should be specified.

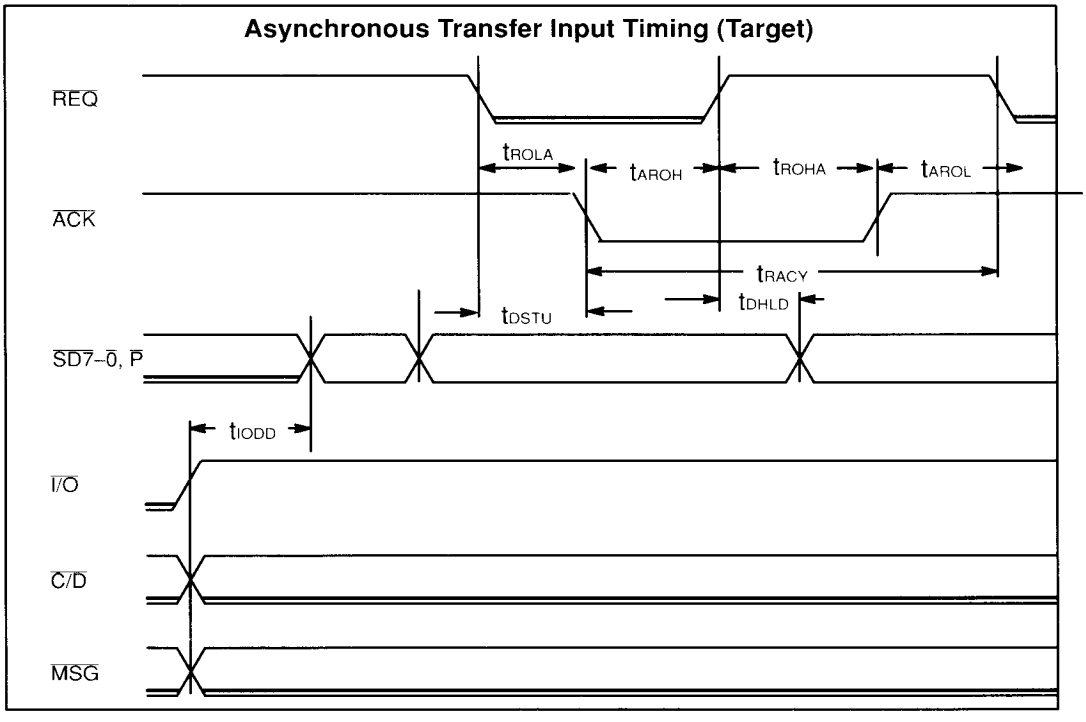
AC CHARACTERISTICS (Continued)

Asynchronous Transfer Input Timing (Initiator)



AC CHARACTERISTICS (Continued)

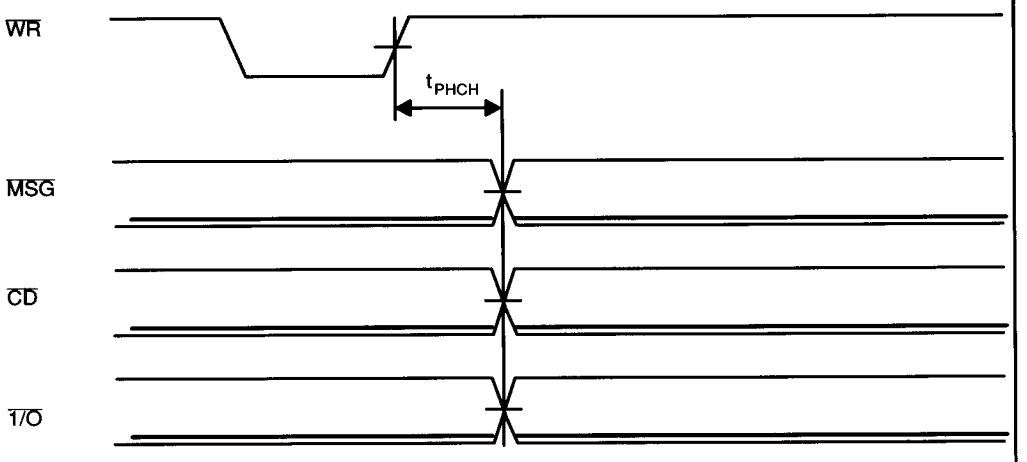
TARGET —Asynchronous Transfer Input					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{I/O}$ High to Data Bus Output Terminate	t_{IODD}			30	ns
Data Bus Valid to $\overline{ACK}$ Low	t_{DSTU}	10			ns
$\overline{REQ}$ High to Data Bus Hold	t_{DHLD}	15			ns
$\overline{REQ}$ Low to $\overline{ACK}$ Low	t_{ROLA}	0			ns
$\overline{ACK}$ Low to $\overline{REQ}$ High	t_{AROH}	10		180	ns
$\overline{REQ}$ High to $\overline{ACK}$ High	t_{ROHA}	0			ns
$\overline{ACK}$ High to $\overline{REQ}$ Low	t_{AROL}	10			ns
$\overline{ACK}$ Low to $\overline{REQ}$ Low	t_{RACY}	$2t_{CLF}$			ns



AC CHARACTERISTICS (Continued)

Transfer Phase Change (Target)					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
From $\overline{WR}$ High to $\overline{MSG}$, C/$\overline{D}$, I/$\overline{O}$ change	t_{PHCH}	10		130	ns

Transfer Phase Change Timing (Target)



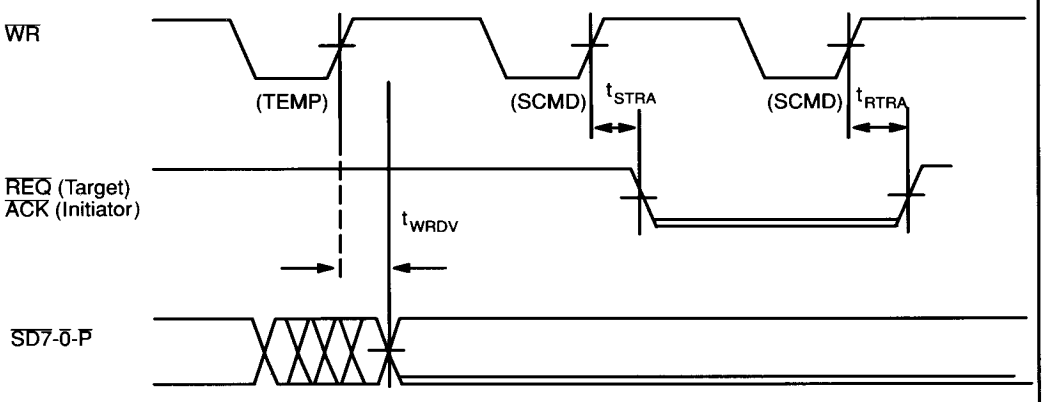
AC CHARACTERISTICS (Continued)

Manual Transfer

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
From $\overline{WR}$ High to Data Bus Valid forTEMP Register	t_{WRDV}			130	ns
From $\overline{WR}$ High to REQ Low, ACK Low for SET ACK/REQ Command	t_{STRA}	$2t_{CLF}$		$3t_{CLF} + 90$	ns
From $\overline{WR}$ High to REQ High, ACK High for RESET ACK/REQ Command	t_{RTRA}	$2t_{CLF}$		$3t_{CLF} + 90$	ns

Note: Timing relationships not shown are the same as those for asynchronous transfers.

Manual Transfer Timing

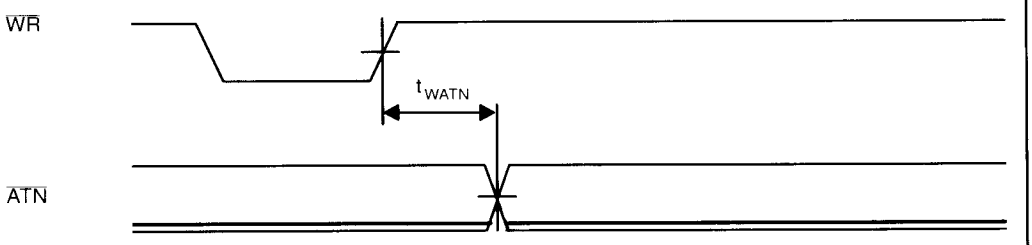


AC CHARACTERISTICS (Continued)

SCSI BUS INTERFACE – ATTENTION CONDITION

INITIATOR - Attention Condition					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
From $\overline{WR}$ High to $\overline{ATN}$ Change (SET/RESET ATN Command)	t_{WATN}	$2t_{CLF}$		$3t_{CLF}$+ 90	ns

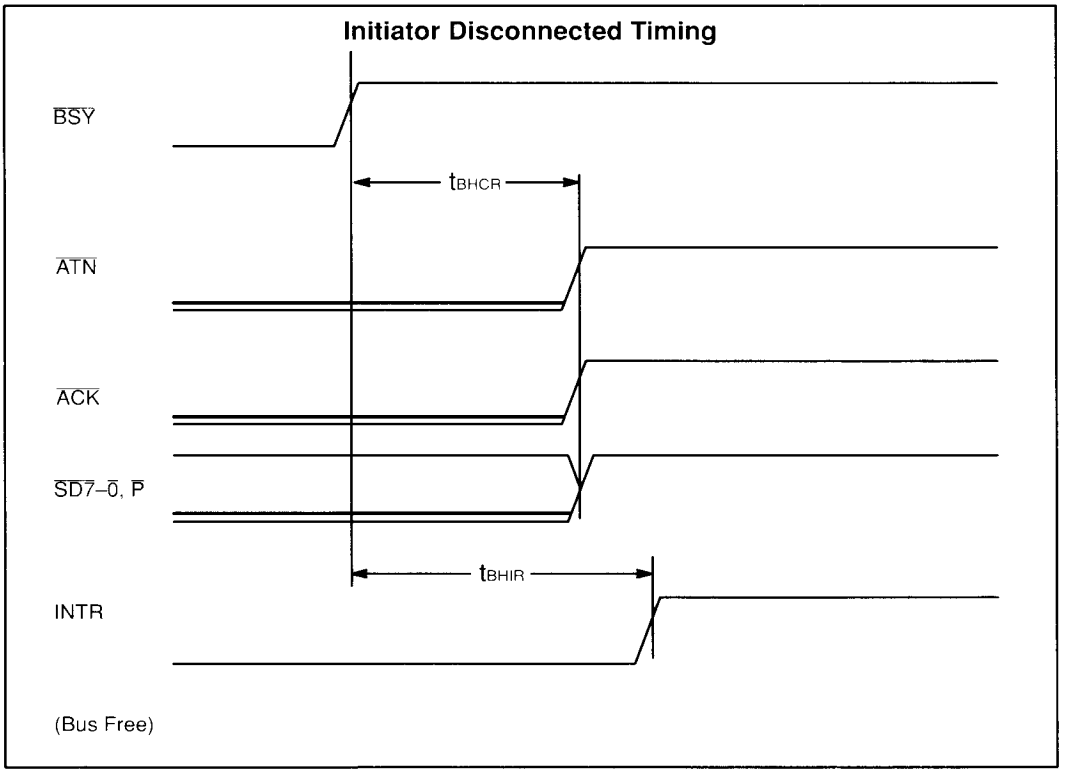
Attention Condition Timing (Initiator)



AC CHARACTERISTICS (Continued)

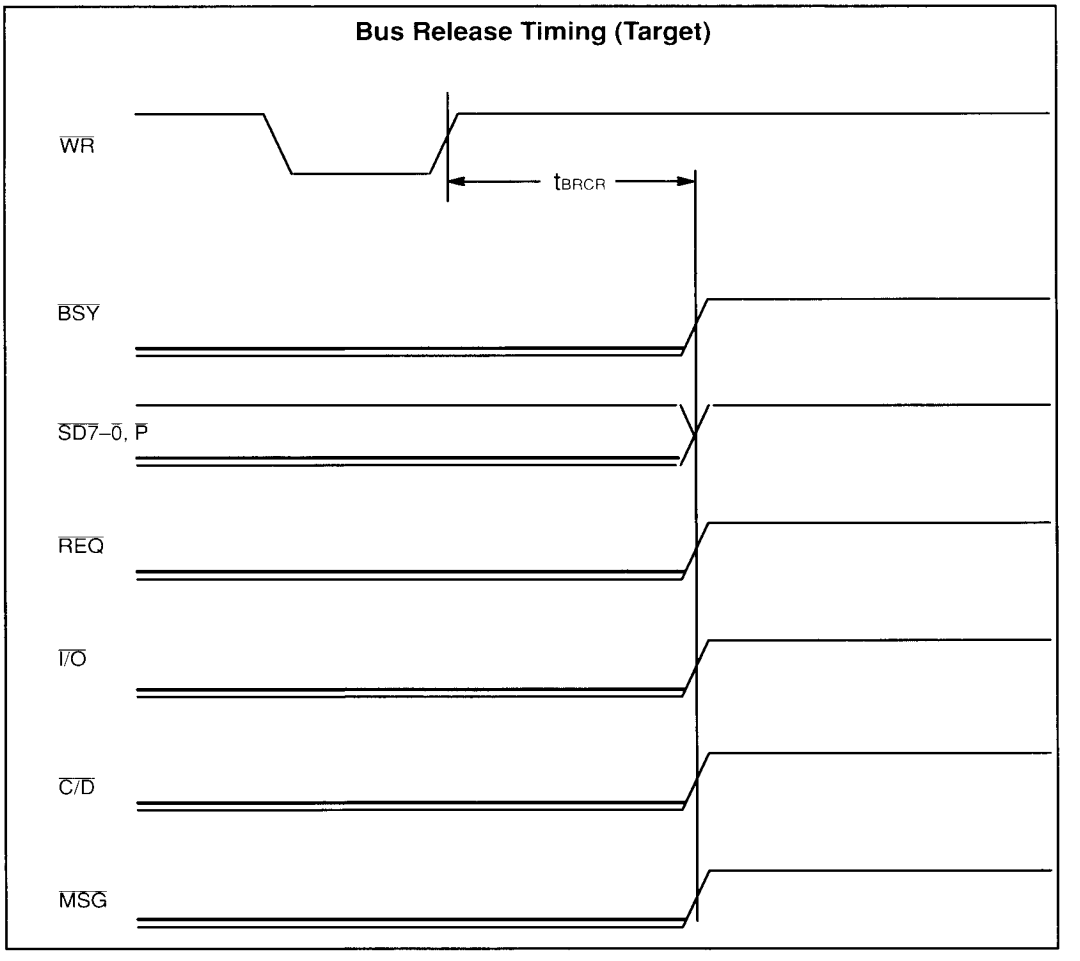
SCSI BUS INTERFACE – BUS FREE

INITIATOR — Bus Free (Disconnection)					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{BSY}$ High to Bus Clear	t_{BHCR}			$5t_{CLF}+140$	ns
$\overline{BSY}$ High to INTR High	t_{BHIR}			$6t_{CLF}+80$	ns



AC CHARACTERISTICS (Continued)

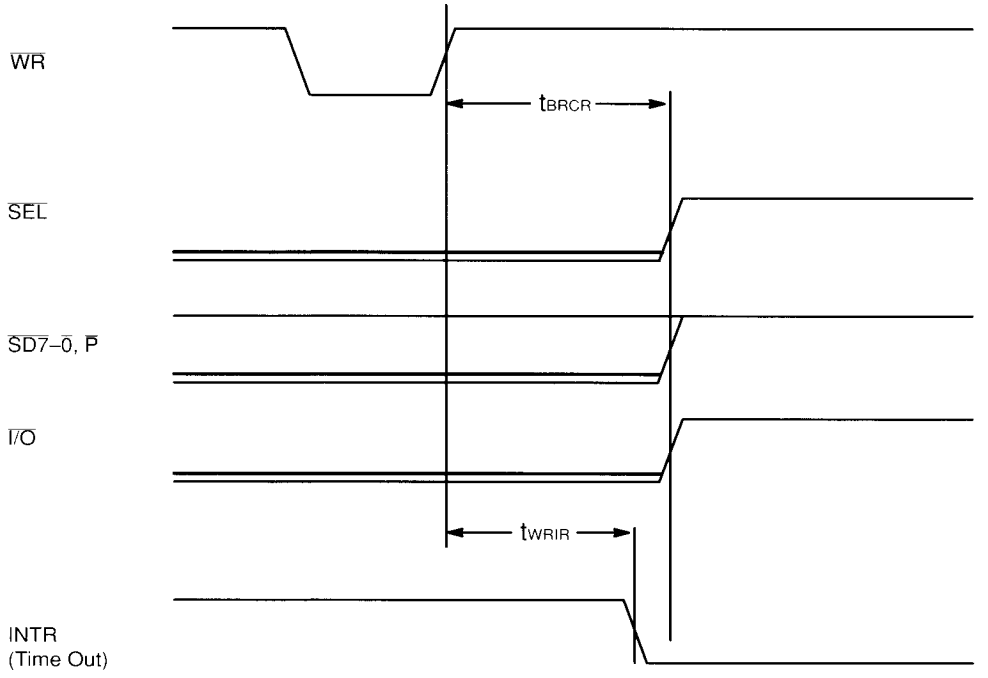
TARGET (Bus Release Command)					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{WR}$ High to Bus Clear (Bus Release Command)	t_{BRCR}			$3t_{CLF}+100$	ns



AC CHARACTERISTICS (Continued)

TERMINATION (Time Out) – Selection and Reselection Phases					
Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{WR}$ High to $\overline{SEL}$, $\overline{SD7–0}$, $\overline{P}$, $\overline{I/O}$ High (Reset Time Out Interruption)	t_{BRCR}			$3t_{CLF}+100$	ns ns
$\overline{WR}$ High to INTR Low	t_{WRIR}			$3t_{CLF}+60$	ns

Timeout Timing (Selection/Reselection Phases)



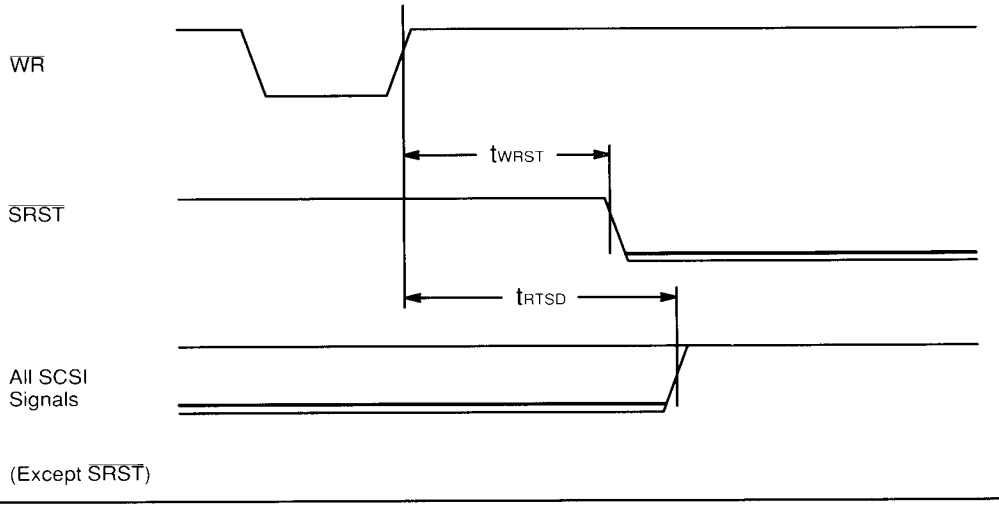
AC CHARACTERISTICS (Continued)

SCSI BUS INTERFACE – RESET CONDITION

$\overline{SRST}$ – Reset Condition (Output)

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{WR}$ High to $\overline{SRST}$ Low (Write "I" to SCMD Bit-4)	t_{WRST}	10		110	ns
Reset Delay	t_{RTSD}			140	ns

$\overline{SRST}$ Signal Transfer Timing



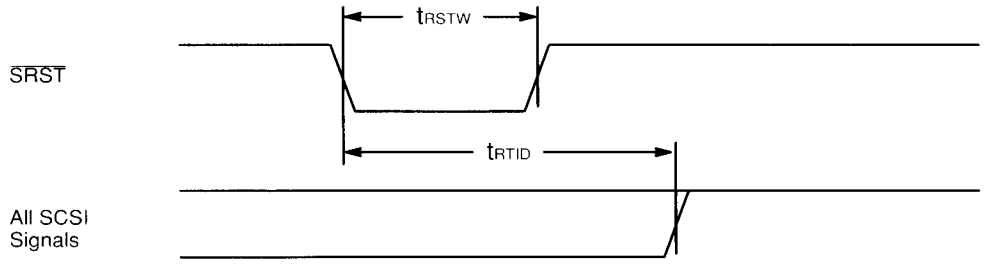
AC CHARACTERISTICS (Continued)

SCSI BUS INTERFACE – RESET CONDITION

$\overline{SRST}$ – Reset Condition (Input)

Parameter	Designator	Values			Unit
		Min.	Typ.	Max.	
$\overline{SRST}$ Pulse Width	t_{RSTW}	$3t_{CLF}$			ns
Reset Delay	t_{RTID}			$4t_{CLF}$+ 200	ns

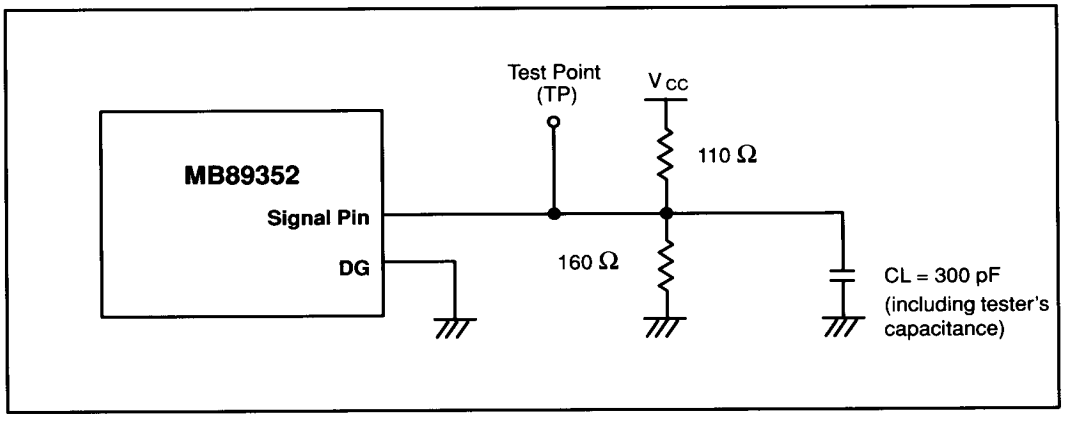
$\overline{SRST}$ Signal Acceptance Timing



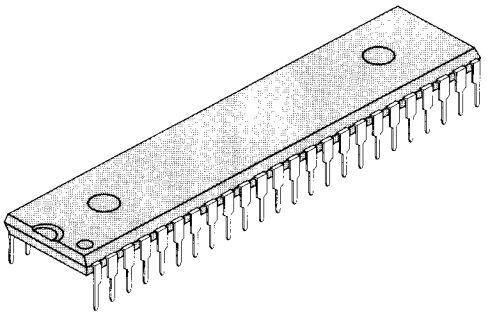
AC CHARACTERISTICS (Continued)

Capacitance			
Parameter	Values		Unit
	Typ.	Max.	
D7 – D0, DP	—	80	pF
DPO, INTR, DREQ	10	30	pF
$\overline{SD7}$ - $\overline{SDO}$, $\overline{SDP}$	—	300	pF
$\overline{SRST}$, $\overline{SEL}$, $\overline{BSY}$, $\overline{I/O}$, $\overline{C/D}$, $\overline{MSG}$, $\overline{REQ}$, $\overline{ACK}$, $\overline{ATN}$	—	300	pF

The AC characteristics of all SCSI bus signal pins are measured on the following test circuit.

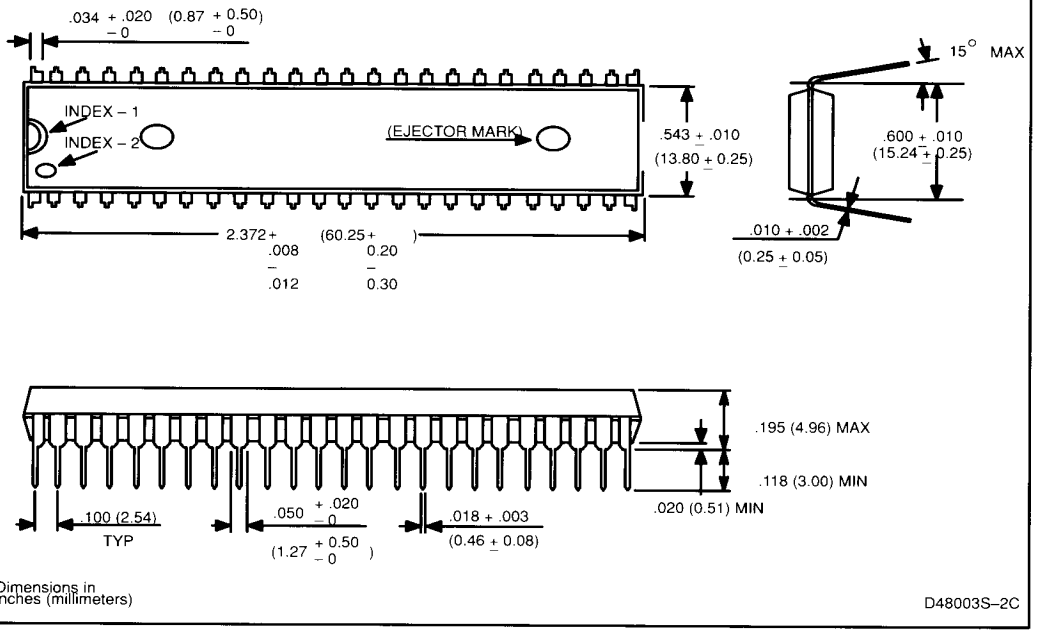


PACKAGE DIMENSIONS



DIP–48P–M02

48–LEAD PLASTIC DUAL–IN–LINE PACKAGE
(CASE NO.: DIP–48P–M02)

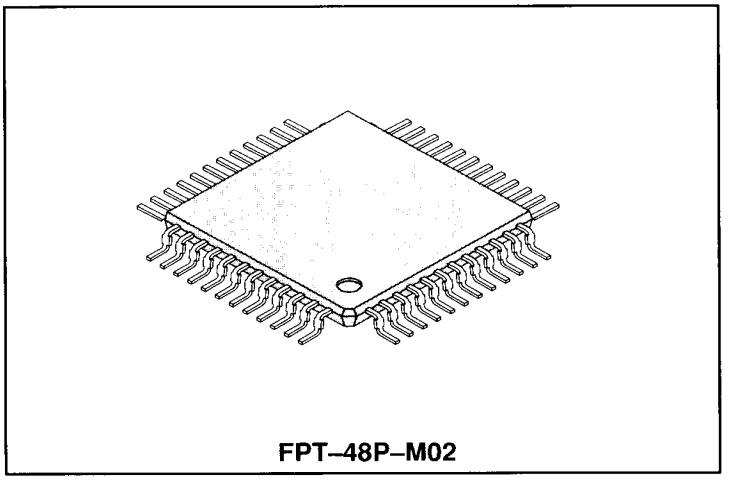


Dimensions in inches (millimeters)

D48003S–2C

PACKAGE DIMENSIONS

48–Lead Plastic Flat Package



FPT–48P–M02